substrate having said impurity precipitation region or of said semiconducting material layer having said impurity precipitation region, to thereby form a conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said conic body is formed.

2. (Amended) The method for manufacturing a semiconductor device according to claim 46, wherein said impurity precipitation region has an etching rate different from that of a main component of said semiconducting material substrate or said semiconducting material layer; and

wherein said impurity precipitation region is formed by thermally treating said impurity introduced into said predetermined position of said semiconducting material substrate or said semiconducting material layer, to precipitate said impurity into a crystal of the semiconducting material substrate or the semiconducting material layer.

B' cont

3. (Amended) The method for manufacturing a semiconductor device according to claim 46, wherein said semiconducting material substrate or said semiconducting material layer comprises silicon; and

wherein said impurity to be introduced is oxygen.

4. (Amended) The method for manufacturing a semiconductor device according to claim 46, wherein the semiconducting material substrate or the semiconducting material layer further comprises a second impurity which bonds to the impurity precipitation region of said first impurity easier than to a material of the semiconducting material substrate or the semiconductive material layer.

5. (Amended) The method for manufacturing a semiconductor device according to

claim 4, wherein each of the semiconducting material substrate and the semiconducting material layer comprises silicon;

wherein the first impurity is oxygen; and

wherein the second impurity is boron.

6. (Amended) The method for manufacturing a semiconductor device according to claim 46, wherein said first impurity is introduced into a predetermined position of said semiconducting material substrate or said semiconducting material layer by a process comprising:

forming an ion implantation mask, which is open at a target conic body forming region and which covers a region other than the target region, on a surface of the semiconducting material substrate or the semiconducting material layer;

ion implanting said first impurity into the semiconducting material substrate or the semiconducting material layer, to obtain an implanted impurity; and

thermally treating said implanted impurity to precipitate it into a crystal of said semiconducting material substrate or said semiconducting material layer, to obtain said semiconducting material substrate having the impurity precipitation region or said semiconducting material layer having the impurity precipitation region.

7. (Amended) The method for manufacturing a semiconductor device according to claim 46, wherein said first impurity is introduced into a predetermined position of said semiconducting material substrate or said semiconducting material layer by a process comprising:

growing the semiconducting material substrate or the semiconducting material layer by an epitaxial method in a direction of a target conic body forming height;

adding gas containing said first impurity to a material gas at a target micro mask

forming height to further grow the semiconducting material substrate or the semiconducting material layer by said epitaxial method; and

removing an epitaxial growth layer containing the impurity while excepting the target conic body forming region.

8. (Amended) A method for manufacturing a semiconductor device, comprising:

introducing a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region;

performing high selectivity anisotropic etching of said semiconducting material substrate having said impurity precipitation region or of said semiconducting material layer having said impurity precipitation region, to thereby form a truncated conic body;

8' cont

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said truncated conic body is formed; and

exposing a top surface of said truncated conic body in the shape of a mortar by etching and performing high selectivity anisotropic etching of a leading end of said truncated conic body to form a truncated conic body having an annular leading end.

9. (Amended) A method for manufacturing a semiconductor device, comprising:

introducing a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region;

performing high selectivity anisotropic etching of said semiconducting material substrate having said impurity precipitation region or of said semiconducting material layer having said impurity precipitation region, to thereby form a conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said conic body is formed;

forming an embedding layer on said etching exposure surface to obtain an embedded conic body;

etching said embedding layer to etch a top of said embedded conic body; and

performing high selectivity anisotropic etching of a top surface of the conic body exposed to the surface into the shape of a mortar extending toward the bottom of the conic body to thereby form a truncated conic body having an annular leading end.

10. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to about 15 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

11. (Amended) A semiconductor device, comprising:

a truncated conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein the truncated conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about several to 30 nm in the vicinity of

its leading end, and an aspect ratio of about 10 or more, and an annular shape at its leading end with a center of a top surface partly removed.

12. (Amended) The semiconductor device according to claim 11, wherein the truncated conic body has its leading end removed in the shape of a mortar from a top face toward the bottom of the truncated conic body to form an annular shape at the leading end.

13. (Amended) A single electron semiconductor device for controlling propagation of a single electron or a small number of electrons, comprising:

a silicon needle conic body protruded on a substrate as at least a part of a propagation passage for said single electron or said small number of electrons.

14. (Amended) The device according to claim 13, further comprising:

a source region and a drain region closely disposed on a side of said silicon needle conic body with said silicon needle conic body intervened therebetween;

B' cont.

wherein said silicon needle conic body is used as a quantum dot; and

wherein between the silicon needle conic body and the source region, between the silicon needle conic body and the drain region, between the source and drain regions, and a space between the silicon needle conic bodies where the silicon needle conic body is formed in multiple numbers, said silicon needle conic body is used as a small tunnel junction to control the propagation of a single or a small number of electrons between the source region and the drain region.

15. (Amended) The single electron semiconductor device according to claim 13, further comprising:

a potential control electrode for controlling a potential in the conic body disposed around the side face of the silicon needle conic body;

wherein the propagation of said single electron or said small number of electrons is

controlled between the vicinity of the bottom and the vicinity of the leading end of the silicon needle conic body by the potential control by the potential control electrode.

16. (Amended) The single electron semiconductor device according to claim 13, further comprising:

a potential control electrode for controlling a potential in the conic body disposed around the side face of the silicon needle conic body;

wherein the vicinity of the side face of the silicon needle conic body is depleted by the potential control electrode to form a quantum wire region at a core of the silicon needle conic body.

17. (Amended) The device according to claim 16, wherein the silicon needle conic body has a conic shape with a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

B1 cont.

18. (Amended) The device according to claim 16, wherein the silicon needle conic body has a truncated conic body with a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more; and

wherein a leading end of the truncated conic body has an annular shape with its center partly removed.

19. (Amended) A single electron semiconductor device for controlling propagation of a single electron or a small number of electrons, comprising:

silicon needle conic bodies protruded on a substrate, and

a conducting material layer formed on the substrate to bury at least the lower portions of the silicon needle conic bodies;

wherein peripheral regions of the silicon needle conic bodies of the conducting material layer function as quantum dots and small tunnel junctions to control the propagation of said single electron or said small number of electrons in a plane direction of the conducting material layer.

20. (Amended) The single electron semiconductor device according to claim 19, wherein each of the silicon needle conic bodies is closely formed in multiple numbers to be arranged in a breadth direction of the conducting material layer; and

wherein the conducting material layer in a region intervened between two adjacent silicon needle conic bodies functions as the quantum dot and a minute channel.

21. (Amended) The single electron semiconductor device according to claim 19, wherein each of the silicon needle conic bodies is closely formed in multiple numbers in a direction along an end of the conducting material layer;

B1 cont

wherein the conducting material layer which is in a region intervened between two adjacent silicon needle conic bodies functions as the quantum dot; and

wherein the conducting material layer which is in a region intervened between the silicon needle conic bodies and an end of the conducting material layer functions as a small tunnel junction.

22. (Amended) The single electron semiconductor device according to claim 19, wherein each of the silicon needle conic bodies is closely formed in multiple numbers in a direction along an end of the conducting material layer;

a depletion layer is formed in the conducting material layer in the peripheral region having the silicon needle conic body at a center; and

a quantum dot and a small tunnel junction are formed in a region between a depletion layer end in the conducting material layer and said end of the conducting material layer.

23. (Amended) The device according to claim 19, wherein the silicon needle conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

24. (Amended) The device according to claim 19, wherein the silicon needle conic body has a truncated conic body with a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more; and

wherein a leading end of the truncated conic body has an annular shape with its center partly removed.

25. (Amended) A semiconductor memory for storing information by accumulating electric charges in a capacitor configuring each memory unit, comprising:

B1 cont

a needle of silicon crystal formed in each memory unit, and a capacitor having the side face of the needle as one of electrodes.

26. (Amended) The semiconductor memory according to claim 25, wherein a switching transistor is formed on a part of the silicon crystal needle to supply the capacitor with electric charges.

27. (Amended) The semiconductor memory according to claim 26, wherein the switching transistor is formed at a base of the silicon crystal needle, and the capacitor is formed at a leading end.

28. (Amended) The semiconductor memory according to claim 26, wherein the switching transistor is formed at a leading end of the silicon crystal needle, and the capacitor is formed below the switching transistor.

29. (Amended) The device according to claim 25, wherein the silicon crystal needle

has a conic shape with a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 ran to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more.

30. (Amended) A method for manufacturing a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons, comprising:

forming an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer, to obtain a single-crystal silicon substrate having an impurity precipitation region or a single-crystal silicon layer having an impurity precipitation region;

performing high selectivity anisotropic etching of said single-crystal silicon substrate having said impurity precipitation region or of said single-crystal silicon layer having said impurity precipitation region to thereby form a silicon needle conic body;

B' cont

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching; and

wherein a top of said silicon needle conic body is said micro mask; and

using the silicon needle conic body as at least a part of a propagation route of the single electron or the small number of electrons of the single electron semiconductor device.

31. (Amended) A method for manufacturing a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons, comprising:

forming an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer, to obtain a single-crystal silicon substrate having an impurity precipitation region or a single-crystal silicon layer having an impurity precipitation region;

performing high selectivity anisotropic etching of said single-crystal silicon substrate having said impurity precipitation region or of said single-crystal silicon layer having said impurity precipitation region to thereby form a silicon needle conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching; and

wherein a top of said silicon needle conic body is said micro mask;

forming a conducting material layer on said single-crystal silicon substrate to bury said silicon needle conic body or at least a lower portion of the silicon needle conic body, and

wherein a peripheral region of the silicon needle conic body of the conducting material layer functions as a quantum dot and a small tunnel junction to control the propagation of said single electron or said small number of electrons in a planar direction of the conducting material layer.

32. (Amended) A semiconductor memory for storing information, comprising:

an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer,

a silicon crystal needle conic body formed in each memory unit on said single-crystal silicon substrate by subjecting said single-crystal silicon substrate having said impurity precipitation region or said single-crystal silicon layer having said impurity precipitation region to high selectivity anisotropic etching;

wherein said impurity precipitation region is used as a micro mask;

wherein said single-crystal silicon substrate or said single-crystal silicon layer have said micro mask at a top; and

a capacitor having a side face of the silicon crystal needle as one of electrodes;

wherein information is stored by accumulating electric charges into said capacitor.

33. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said semiconductor device is a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons;

B1 cont.

wherein said conic body is a silicon needle conic body protruded on said substrate as at least a part of a propagation passage for the single electron or the small number of electrons.

35. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

B2

wherein said semiconductor device is a single electron semiconductor device for controlling propagation of a single electron or a small number of electrons;

wherein said conic body is a silicon needle conic body protruded on said substrate;

wherein said semiconductor device further comprises a conducting material layer formed on said substrate to bury at least a lower portion of the silicon needle conic body;

wherein peripheral regions of the silicon needle conic bodies of the conducting material layer are functioned as quantum dots and small tunnel junctions to control the propagation of a single electron or a small number of electrons in a plane direction of the conducting material layer.

36. (Amended) The semiconductor device according to Claim 11, which is a single

electron semiconductor device for controlling propagation of a single electron or a small number of electrons;

wherein said conic body is a silicon needle conic body protruded on said substrate;

wherein said semiconductor device further comprises a conducting material layer formed on said substrate to bury at least a lower portion of the silicon needle conic body;

wherein peripheral regions of the silicon needle conic bodies of the conducting material layer are functioned as quantum dots and small tunnel junctions to control the propagation of a single electron or a small number of electrons in a plane direction of the conducting material layer.

37. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

B2 cont

wherein said conic body has a radius of curvature of several to more than 10 nm in the vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said semiconductor device is a semiconductor memory for storing information by accumulating electric charges in a capacitor configuring each memory unit,

wherein said semiconductor memory further comprises a needle of silicon crystal formed in each memory unit, and a capacitor having the side face of the needle as one of electrodes.

38. (Amended) A semiconductor device, comprising:

a conic body formed on a semiconducting material substrate or a semiconducting material layer;

wherein said conic body has a radius of curvature of several to more than 10 nm in the

vicinity of its leading end or a diameter of about 10 nm to 30 nm in the vicinity of its leading end, and an aspect ratio of about 10 or more;

wherein said semiconductor device is a semiconductor memory for storing information,

wherein said semiconductor memory comprises

an impurity precipitation region in a single-crystal silicon substrate or a single-crystal silicon layer,

said conic body which is a silicon crystal needle conic body formed in each memory unit on the substrate by subjecting the silicon substrate or the silicon layer to high selectivity anisotropic etching with the impurity precipitation region used as a micro mask, the silicon precipitation region having the micro mask at a top, and

a capacitor having a side face of the silicon crystal needle as one of electrodes,

wherein information is stored by accumulating electric charges into the capacitor.

Please add the following new Claims:

39. (New) The semiconductor device according to Claim 10, wherein said conic body has a radius of curvature of several to 10 nm in the vicinity of its leading end.

40. (New) The semiconductor device according to Claim 11, wherein said truncated conic body has a radius of curvature of several to 10 nm in the vicinity of its leading end.

41. (New) The semiconductor device according to Claim 17, wherein said silicon needle conic body has a radius of curvature of several to 10 nm in the vicinity of its leading end.

42. (New) The semiconductor device according to Claim 18, wherein said silicon needle conic body has a radius of curvature of several to 10 nm in the vicinity of its leading end.

43. (New) The semiconductor device according to Claim 23, wherein said silicon needle conic body has a radius of curvature of several to 10 nm in the vicinity of its leading end.

44. (New) The semiconductor device according to Claim 24, wherein said silicon needle conic body has a radius of curvature of several to 10 nm in the vicinity of its leading end.

45. (New) The semiconductor device according to Claim 29, wherein said silicon crystal needle has a radius of curvature of several to 10 nm in the vicinity of its leading end.

46. (New) A method for manufacturing a semiconductor device according to claim 10, comprising:

B3 cont

introducing a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region; and

performing high selectivity anisotropic etching of said semiconducting material substrate having said impurity precipitation region or of said semiconducting material layer having said impurity precipitation region, to thereby form a conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said conic body is formed.

47. (New) A method for manufacturing a semiconductor device according to claim 11, comprising:

introducing a first impurity into a predetermined position of a semiconducting

material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region;

performing high selectivity anisotropic etching of said semiconducting material substrate having said impurity precipitation region or of said semiconducting material layer having said impurity precipitation region, to thereby form a truncated conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said truncated conic body is formed; and

B3 cont

exposing a top surface of said truncated conic body in the shape of a mortar by etching and performing high selectivity anisotropic etching of a leading end of said truncated conic body to form a truncated conic body having an annular leading end.

48. (New) A method for manufacturing a semiconductor device according to claim 11, comprising:

introducing a first impurity into a predetermined position of a semiconducting material substrate or a semiconducting material layer, to obtain a semiconducting material substrate having an impurity precipitation region or a semiconducting material layer having an impurity precipitation region;

performing high selectivity anisotropic etching of said semiconducting material substrate having said impurity precipitation region or of said semiconducting material layer having said impurity precipitation region, to thereby form a conic body;

wherein said impurity precipitation region is used as a micro mask during said anisotropic etching;

wherein said micro mask is a top of an etching exposure surface on which said anisotropic etching is performed and on which said conic body is formed;

forming an embedding layer on said etching exposure surface to obtain an embedded conic body;

B3 concl

etching said embedding layer to etch a top of said embedded conic body; and

performing high selectivity anisotropic etching of a top surface of the conic body exposed to the surface into the shape of a mortar extending toward the bottom of the conic body to thereby form a truncated conic body having an annular leading end.

BASIS FOR THE AMENDMENT

Claims 1-38 have been amended to recite proper claim language.

The amendment of Claim 1 is further supported at page 5, 1st full paragraph and by Figure 2.

The amendment of Claim 8 is further supported at page 35, lines 23-24 and by Figure 9.

The amendment of Claim 10 is further supported at page 26, lines 15-19. Although there is no explicit description of the upper limit of the radius of curvature being about 15 nm, there is an explicit description of the diameter of the leading portion of a conic body being 10-30 nm at page 26, lines 15-19. Therefore, when the conic body is a cone as exemplified in the preferred embodiments, the radius of curvature is consequently 15 nm.

Claims 33, 35, 37 and 38 have been rewritten in independent form to include the limitations of amended Claim 10.

New Claims 39-48 have been added.

New dependent Claims 39-45 are supported by Claims 10, 11, 17, 18, 23, 24 and 29

as originally filed, respectively.

New Claim 46 is supported by Claim 1 as originally filed.

New Claim 47 is supported by Claim 8 as originally filed.

New Claim 48 is supported by Claim 9 as originally filed.

No new matter is believed to have been added by entry of this amendment. Entry and favorable reconsideration are respectfully requested.

Upon entry of this amendment **Claims 1-48 will now be active** in this application. Claims 12-29 and 32 stand withdrawn from further consideration as being drawn to non-elected subject matter.

REQUEST FOR RECONSIDERATION

Applicants wish to thank Examiner Garcia and Supervisory Examiner Fourson for their helpful and courteous discussion with Applicants' Representative on October 29, 2002. During this discussion it was suggested to amend Claim 10 to claim a radius of curvature of several to about 15 nm to distinguish from Kirk et al. (Support for this amendment has been discussed in detail above.) The Examiner indicated that based on the amendment of Claim 10, she will reconsider her position in regard to Kirk et al.

In addition, Applicants appreciate:

1.) the indication of allowability of Claim 11 if rewritten to overcome the rejection under 35 U.S.C. §112, 2nd paragraph,

2.) the indication of allowability of Claims 35, 36 and 38 if rewritten to overcome the rejection under 35 U.S.C. §112, 2nd paragraph, and to include all of the limitations of the base claim and any intervening claims, and

3.) the indication of allowability of Claims 33, 34 and 37 if rewritten to include all of